IN THE CLAIMS

Please cancel claims 2-6, 8, 11-20, 22, and 25 without prejudice.

1. (Original) A method, comprising:

providing at least three elements, including a first element and a last element, each element having an associated parameter;

providing a first identifier for the first element;

for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to produce a transform;

saving the transform; and

for a second sequential execution of the elements, performing a second operation on the transform to produce a last identifier associated with the last element.

2-6 (Cancelled)

7. (Original) The method of claim 1, wherein performing the second operation includes:

shifting the first identifier to produce a shifted identifier; and

performing an exclusive OR operation on the shifted identifier and the transform to produce the last identifier.

8. (Cancelled)

9. (Original) The method of claim 1, wherein the at least three elements are branch instructions in an instruction execution pipeline.

10. (Original) The method of claim 1, further comprising:

using the last index to access a location in a prediction array; and

using a content of said location to predict a decision status of the last element.

11-20 (Cancelled)

21. (Original) A circuit, comprising:

a register;

a data shifting circuit having an input coupled to an output of the register;

an exclusive OR circuit having a first input coupled to an output of the data shifting circuit;

an array coupled to a second input of the exclusive OR circuit to transfer transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit; and

a prediction logic circuit coupled to an output of the exclusive OR circuit.

22. (Cancelled)

23. (Original) The circuit of claim 21, wherein the data shifting circuit includes a plurality of inputs coupled to the output of the register to shift data from the register by a selected number of bits.

24. (Original) A computer system comprising:

an instruction execution pipeline;

a transform generation circuit coupled to the instruction execution pipeline and including:

a register;

a data shifting circuit having an input coupled to an output of the register;

an exclusive OR circuit having a first input coupled to an output of the data shifting circuit;

an array coupled to a second input of the exclusive OR circuit to transfer transform data to the exclusive OR circuit, and further coupled to the data shifting circuit to transfer data shift information to the data shifting circuit; and

a prediction logic circuit coupled to an output of the exclusive OR circuit.

25. (Cancelled)

26. (Original) The computer system of claim 24, wherein the data shifting circuit includes a plurality of inputs coupled to the output of the register to shift data from the register by a selected number of bits.

27. (Original) A machine-readable medium having stored thereon instructions, which when executed by at least one processor cause said at least one processor to perform:

providing at least three elements, including a first element and a last element, each element having an associated parameter;

providing a first identifier for the first element;

for a first sequential execution of the at least three elements, performing a first operation on the first identifier and at least one of the parameters to produce a transform;

saving the transform;

for a second sequential execution of the elements, performing a second operation on the transform to produce a last identifier associated with the last element;

using the last identifier to access a location in a prediction array; and

using a content of said location to predict a decision status of the last element.